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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,218	07/02/2001	Brian Gaudet	0023-0036	8537

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EXAMINER	
PHAN, TRI H	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,218	GAUDET, BRIAN	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-24 and 26-33* is/are pending in the application.

4a) Of the above claim(s) *4 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-3,5-24 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Arguments

1. This Office Action is in response to the Response/Amendment filed on June 6th, 2005. Claims 4 and 25 are now canceled and new claims 30-33 are added. Claims 1-3, 5-24, and 26-33 are now pending in the application.

Claim Objections

2. Claims 15 and 16 are objected to because of the following informalities:

In claim 15, line 2, the word "a" right in front of the term "first packets" should be correct to --- the ---.

Same objection for claim 16, line 2, the word "a" right in front of the term "first packets" should be correct to --- the ---.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 7-11, 13-19, 21-24, 26-27, 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gaudet et al.** (U.S.6,421,348; hereinafter refer as '**Gaudet**').

- In regard to claims 1 and 7, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *packet processing system* ('switched network 100' in fig. 1) *and method for converting the first data path* ('external PHYs 112/162' in fig. 1) *carrying P packets per processing cycle to the second data path* ('external PHYs 112/162' or 'switch data bus 150' in fig. 1) *carrying Q packets per processing cycle* (for example see fig. 1; col. 3, lines 64-67), *wherein* $Q < P$ (for example see col. 4, lines 58-65; col. 5, lines 57-59; where the packet "P" is converted into frame data, which is further divided into 48-bit cells "Q"), *which comprises receiving the P packets during the first processing cycle on the first data path* (for example see col. 4, lines 55-58), *storing the P packets in a queue* ('port FIFOs 703-711'; col. 8, lines 12-17), *shifting first data from the queue into the shift register* ('bus FIFO 712' in fig. 7; col. 8, lines 17-19; although, 'bus FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'bus FIFO' is an obvious form of "*shift register*", which provides function such as holding the SOF cells ready for transmission, e.g. "*shift register*", and transmits these cells over the switch bus as disclosed in figs. 7, 14A-B; col. 12, lines 59-61), *selectively retrieving data from the shift register until the first set of Q packets of the P packets is retrieved, wherein the data from the shift register is selectively retrieved based on the determination of whether the data comprises one of an end-of-packet indicator, a data field, or a start-of-packet indicator* (wherein the bus FIFO continues

transmitting cells until all cells have been transmitted, e.g. "*based on the determination of whether the data comprises data field*" or 'cell to transmit', as disclosed in step 516-518 of fig. 5; col. 5, lines 3-6; col. 6, line 62 through col. 7, line 2; under the control of the buffer manager 140 "*control unit*" disclosed in col. 4, lines 38-42) *and sending the set of Q packets on the second data path* ('switch bus'; col. 5, lines 4-5; col. 6, lines 62-63) *during the first processing cycle.*

- Regarding claim 2, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), **Gaudet** further discloses about *shifting second data* (cells which belong to the incoming frame) *from the queue into the shift register* ('bus FIFO'), *selectively retrieving data from the shift register until a second set of Q packets of the P packets is retrieved* (for example see col. 7, lines 28-41; testing for the EOF) *and sending the second set of Q packets on the second data path during a second processing cycle* (for example see col. 7, lines 45-48).

- In regard to claims 8 and 13, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *packet processing system* ('switched network 100' in fig. 1) *and method for converting the first data path* ('external PHYs 112/162' in fig. 1) *carrying P packets per processing cycle to the second data path* ('external PHYs 112/162' or 'switch data bus 150' in fig. 1) *carrying Q packets per processing cycle* (for example see fig. 1; col. 3, lines 64-67), *wherein* $Q < P$ (for example see col. 4, lines 58-65; col. 5, lines 57-59; where the packet "P" is converted into frame data, which is further divided into 48-bit cells "Q"; and therefore, Q

< P), *which comprises receiving the P packets during a first processing cycle on the first data path* (for example see col. 4, lines 55-58), *storing the P packets in a queue* ('port FIFOs 703-711'; col. 8, lines 12-17), *shifting first data from the queue into the shift register* ('bus FIFO 712' in fig. 7; col. 8, lines 17-19; although, 'bus FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'bus FIFO' is an obvious form of "*shift register*", which provides function such as holding the SOF cells ready for transmission, e.g. "*shift register*", and transmits these cells over the switch bus as disclosed in figs. 7, 14A-B; col. 12, lines 59-61), *determining whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator* (wherein the bus FIFO continues transmitting cells until all cells have been transmitted, e.g. "*data field*" or 'cell to transmit', as disclosed in step 516-518 of fig. 5; col. 5, lines 3-6; col. 6, line 62 through col. 7, line 2; under the control of the buffer manager 140 "*control unit*" disclosed in col. 4, lines 38-42) *and, based on the determination, sending the first set of Q packets on the second data path during the first processing cycle* ('switch bus'; col. 5, lines 4-5; col. 6, lines 62-63).

- Regarding claim 9, in addition to features in base claim 8 (see rationales pertaining the rejection of base claim 8 discussed above), **Gaudet** further discloses about *shifting second data* ('additional cells') *of the P packets from the queue into the shift register* (for example see figs. 5-6; col. 6, lines 63-66), *determining whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator* (wherein the bus FIFO continues transmitting cells until all cells have been transmitted, e.g. "*data field*" or 'cell to transmit', as disclosed in step 516-518 of fig. 5; col. 4, line 65 through col. 5, line 6; col. 6, line

62 through col. 7, line 2) *and, based on the determination* (where the number of cells are exceeded the drain threshold), *sending the second set of Q packets on the second data path during the second processing cycle* ('switch bus'; col. 5, lines 1-6).

- In regard to claims 14 and 21, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *packet processing system* ('switched network 100' in fig. 1) *and method for processing packets* (for example see col. 3, line 63 through col. 4, line 1), *which comprises the first data path configured to receive P packets* ('external physical layer 112' @ fig. 1; col. 4, lines 55-58), *the second data path* ('switch data bus 150' in fig. 1) *configured to carry Q packets* ('48-bit cells') *during the first processing cycle, wherein* $Q < P$ (for example see col. 4, lines 58-65; col. 5, lines 57-59; where the packet "P" is converted into frame data, which is further divided into 48-bit cells "Q"; and therefore, $Q < P$), *the processing unit* ('data exchanger') *configured to convert the received P packets* ('packets') *on the first data path to the first set of Q packets* ('48-bit cells') *on the second data path during the first processing cycle and convert the received P packets on the first data path to a second set of Q packets on the second data path during a second processing cycle* (for example see col. 4, line 58 through col. 5, line 6; wherein the data exchanger monitor for the SOF in order to divide the frame data into cells for loading into the bus FIFO), *a first processing device* ('data exchanger') *configured to process the first set of Q packets on the second data path during the first processing cycle and process the second set of Q packets on the second data path during the second processing cycle* (for example see steps 516-518 @ fig. 5; col. 6, line 62 through col. 7, line 2; steps 616-622 @ fig. 6; col. 7,

lines 41-48; wherein the data exchanger monitors the EOF contained in the received cell and if the cell does not contain an EOF, the data exchanger continues to load cells).

- Regarding claims 15-17, in addition to features in base claim 14 (see rationales pertaining the rejection of base claim 14 discussed above), **Gaudet** further discloses about *shifting the first quantity of data of the plurality of packets into the shift register* ('bus FIFO 712' in fig. 7; col. 8, lines 17-19; although, 'bus FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'bus FIFO' is an obvious form of "*shift register*", which provides function such as holding the SOF cells ready for transmission, e.g. "*shift register*"), *selectively retrieving data from the shift register until the first packet* ('SOF') *is retrieved* (for example see col. 4, lines 63-64) *and sending the first packet on the first data path during the first processing cycle* (for example see col. 4, lines 64-66). **Gaudet** further discloses about *selectively retrieving data from the shift register until the second packet is retrieved* ('EOF') *and sending the second packet on the second data path during the first processing cycle* (for example see col. 7, lines 41-48). **Gaudet** further discloses about *wherein the data from the shift register is selectively retrieved based on the determination of whether the data comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator* (for example see col. 4, line 63 through col. 5, line 6; col. 6, line 63 through col. 7, line 2; col. 7, lines 41-48).

- In regard to claims 22 and 29, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *packet processing system* ('switched network 100' in fig.

1) *and method for processing a plurality of packets using a packet per cycle processing device* (for example see packet 102a @ fig. 1), *which comprises receiving the plurality of packets during the first processing cycle* (for example see col. 4, lines 55-58), *storing the plurality of packets in the queue* ('port FIFO'; for example see col. 4, lines 58-62; where the port FIFO is disclosed in col. 8, lines 12-17), *shifting the first quantity of data* ('48-bit cells') *of the plurality of packets from the queue into the shift register* ('bus FIFO 712' in fig. 7; col. 8, lines 17-19; although, 'bus FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'bus FIFO' is an obvious form of "*shift register*", which provides function such as holding the SOF cells ready for transmission, e.g. "*shift register*"), *selectively retrieving data from the shift register until the first packet of the plurality of packets is retrieved, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises at least one of an end-of-packet indicator, a data field, or a start-of-packet indicator* (wherein the bus FIFO continues transmitting cells until all cells have been transmitted, e.g. "*data field*" or 'cell to transmit', as disclosed in step 516-518 of fig. 5; col. 5, lines 3-6; col. 6, line 62 through col. 7, line 2) *and processing the retrieved first packet during the first processing cycle* (for example see col. 5, lines 4-5; col. 6, lines 62-63).

- Regarding claim 23, in addition to features in base claim 22 (see rationales pertaining the rejection of base claim 22 discussed above), **Gaudet** further discloses about *selectively retrieving data from the shift register until the second packet* ('cell contains an EOF') *of the*

plurality of packets is retrieved (for example see col. 7, lines 41-46) *and processing the retrieved second packet during the second processing cycle* (for example see col. 7, lines 46-48).

- In regard to claims 18-19 and 26-27, in addition to features in base claim 14 (see rationales pertaining the rejection of base claim 14 discussed above), **Gaudet** further discloses *wherein the processing device* ('data exchanger') *that is configured to process only one packet* (packet 102a @ fig. 1) *per processing cycle processes the first packet on the second data path during the first processing cycle* (for example see col. 4, line 55 through col. 5, line 6) *and wherein the processing device processes the second packet on the second data path during the second processing cycle* (for example see col. 7, line 41-48).

- Regarding claims 3, 10 and 24, in addition to features in base claims 1 or 8 or 22 (see rationales pertaining the rejection of base claims 1 or 8 or 22 discussed above), **Gaudet** further discloses *wherein the queue comprises the first-in-first-out 'FIFO' queue* ('port FIFO'; for example see col. 8, lines 12-14).

- In regard to claims 5 and 11, in addition to features in base claims 1 or 8 (see rationales pertaining the rejection of base claims 1 or 8 discussed above), **Gaudet** further discloses *wherein the second path* (switch bus) *is coupled to a processing device configured to process a maximum of Q packets* (when the bus FIFO exceeds the drain threshold or the maximum of cells can be hold in the bus FIFO) *per processing cycle* (for example see col.5, lines 1-6).

- Regarding claim 30, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *method, which comprises receiving multiple data units* ('frame data'; for example see col. 4, lines 55-62) *during the first processing cycle on the first data path* ('external PHYs 112/162' in fig. 1), *wherein each of the data units comprises segments, the segments comprising the start segment* ('SOF' or 'SFD'@ fig. 2), *one or more data segments* ('data'@ fig. 2) *and the end segment* ('EOF' or 'EFD'@ fig. 2); *storing each of the multiple data units in the queue* ('port FIFOs 703-711'; col. 8, lines 12-17), *shifting first multiple segments* ('48-bit cells') *from the multiple data units into the shift register* ('receive FIFO 712'; col. 4, lines 63-66; although, 'receive FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'receive FIFO' is an obvious form of "*shift register*", which provides function such as holding the cells ready for transmission as disclose in fig. 7, e.g. "*shift register*"), *selectively retrieving segments from the shift register until an end segment is retrieved* (for example see col. 7, lines 41-45) *and sending the retrieved segments on a second data path* ('transmit FIFO/port') *during the first processing cycle* (for example see col. 7, lines 45-50).

- In regard to claim 31, in addition to features in base claim 30 (see rationales pertaining the rejection of base claim 30 discussed above), **Gaudet** further discloses *shifting second multiple segments from one of the multiple data units into the shift register* ('receive FIFO 712'; col. 4, lines 63-66; although, 'receive FIFO' instead of "*shift register*" is used in **Gaudet**'s teaching, it is obvious that one of ordinary skill in the art would recognize that the 'receive FIFO' is an obvious form of "*shift register*", which provides function such as holding the cells

ready for transmission as disclose in fig. 7, e.g. "*shift register*"), *selectively retrieving segments from the shift register until another end segment is retrieved* (for example see col. 7, lines 41-45) *and sending the retrieved segments on the second data path during the second processing cycle* (for example see col. 7, lines 45-50).

- Regarding claim 32, in addition to features in base claim 30 (see rationales pertaining the rejection of base claim 30 discussed above), **Gaudet** further discloses *wherein selectively retrieving segments from the shift register further comprises identifying the start segment* ('SOF') *in the shift register* (for example see fig. 11; col. 10, line 67 through col. 11, lines 2) *and selectively retrieving segments in the shift register* (for example see col. 11, lines 19-21) *between the start segment and the retrieved end segment* ('EOF').

- In regard to claim 33, **Gaudet** discloses in Figs. 1-14B and in the respective portions of the specification about the *method, which comprises receiving multiple data units* ('frame data'; for example see col. 4, lines 55-62) *during the first processing cycle on the first path* ('external PHYs 112/162' in fig. 1), *wherein each of the multiple data units comprises segments, the segments comprising a start segment* ('SOF' or 'SFD'@ fig. 2), *one or more data segments* ('data'@ fig. 2), *and an end segment* ('EOF' or 'EFD'@ fig. 2), *storing the multiple data units* (col. 8, lines 12-17), *successively analyzing each segment of at least a portion of the stored data units to identify the end segment* (for example see col. 7, lines 41-45) *and sending each data unit of the multiple data units that corresponds to one of the identified end segment on the second path during the first processing cycle* (for example see col. 7, lines 45-50).

5. Claims 6, 12, 20 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gaudet et al.** (U.S.6,421,348) in view of **Wakeman et al.** (U.S.5,790,786; hereinafter refer as '**Wakeman**').

- In regard to claims 6, 12, 20 and 28, **Gaudet** discloses the system and method of claims 1 or 8 or 14 or 22 as disclosed in part 4 above in this office action. However, **Gaudet** lacks what **Wakeman** discloses, wherein the processing device comprises the Cyclical Redundancy Checker 'CRC' (for example see fig. 2A; col. 2, lines 57-62). It would have been obvious to one with ordinary skill in the art at the time of invention to include the "*Cyclical Redundancy Checker*" with the system of claims 1 or 8 for the purpose of checking errors for the received and transmitted packets from receive/transmit data path with reliable. The motivation being that providing reliable for the transmission packets onto data path.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kozaki et al. (U.S.5,365,519), **McBrien, Gregory J.** (U.S.4,556,850) and **Gulick et al.** (U.S.4,907,225) are all cited to show devices and methods for improving system and method for improving the transmission data in the telecommunication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (571) 272-3074. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on (571) 272-3126.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(571) 273-8300

Hand-delivered responses should be brought to Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tri H. Phan
September 30, 2005

BRIAN NGUYEN
PRIMARY EXAMINER